

Appl. No : 10/074,881  
Amdt. dated : 09/30/03  
Reply to Office Action of 09/16/03

Amendments to the Specification:

1) page 8, last paragraph, page 9, first paragraph, please replace this text with the following amended text:

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A' As a first step in the creation of the EPROM device, a layer (not shown) of sacrificial silicon oxide is grown on the surface of the n-type substrate to clean the edge of the field oxide regions 14, that is to remove or limit the extend of the "bird's beak" (regions of field oxide that laterally extend from the body of the field oxide region) that is typically part of the field oxide regions.

The layer of sacrificial silicon oxide is then stripped before growth of the tunnel oxide (layer 16) in the active regions of the surface of the substrate. The thin layer 16 of tunnel oxide is formed over the exposed surface of the substrate 10 including the surface of the field oxide layers 14.

A layer of polysilicon (poly 1) is deposited over the surface of the layer 16 of gate oxide, this layer of poly 1 is

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selectively etched and forms the layers 18 that ~~functions~~  
function as the floating gates of the EPROM device.

G<sup>1</sup> A layer 20, of for instance inter-polysilicon ONO, is deposited over the surface of the floating gates 18. The gate structure of the EPROM devices is completed by the overlying layer 22 of poly 2, which forms the control gate that runs in an X-direction of the memory array interconnecting a plurality of control gates in that direction.

The self-aligned floating gates 18 are formed at the same time by selective etching. A p-type implant is performed into the surface of the substrate 10 forming the p-type source regions (not shown) in the surface of the substrate 10. The p-type implanted ions can be further driven into the surface of the substrate to make the source regions deep regions. Ion implants of p-type are performed into the substrate to form (shallower) p-type doped drain regions (not shown).

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2) page 9, second paragraph, please replace this text with the following amended text:

Q2 The structure of the cross section that is shown in Fig. 1 can be further completed by depositing an insulating layer over the structure that also covers the gate control strips electrode 22. Openings are made in this layer of insulation above the drain regions.

Electrical contact is established with the drain regions of the structure by means of a plurality of metal strips that are created in the Y-direction. The source region is contacted (not shown) by metal lines that have been extended in the X-region of the array. A coating of insulation is deposited to overly the metal strips that are created in the Y-direction in order to establish contact with the drain regions of the structure.

3) page 12, last paragraph, page 13, first paragraph, please replace this text with the following amended text:

Q3 For prior art applications that are aimed at measuring the electron charge that is incurred during the processing of semiconductor devices, a large metal area ~~has been~~ is created over ~~surface of the~~ a substrate ~~[[and]]~~ in combination with a gate ~~electrodes~~ electrode. This large metal surface collects the

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Q3  
electron charge since it functions as an antenna of large size.  
The large antenna is connected to the gate electrode,  
influencing the electrical characteristics of the gate  
electrode. By then reading the threshold voltage of the gate  
electrode, the amount of charging that has taken place can be  
determined.

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4) page 13, last paragraph, page 14, first paragraph, please  
replace this text with the following amended text:

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Q4  
The ~~monitor~~ monitoring wafer starts with an n-type substrate  
over the surface of which first regions of field isolation are  
created.

It is well known in the art that in order to ~~created~~ create  
high-performance semiconductor devices, these devices are being  
formed in or on the surface of a substrate using increasingly  
higher device densities and smaller feature sizes.

Continuing device shrinkage and increased device density  
~~presents~~ present new problems in the creation of the devices.  
One such problem is the necessity of building an efficient and

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reliable process to separate active devices that function on the current miniaturized scale.

A4 One method previously used is termed Local Oxidation of Silicon (LOCOS) process. The LOCOS process involves the use of a temporary patterned nitride layer, which is used as a protection or resistant area to cover the future active areas during the subsequent field oxidation process in forming CMOS gate structures. LOCOS is a non-planarized isolation technology in which a trench is etched into the electrically active silicon and filled with oxide

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5) page 22, last paragraph, page 23, first paragraph, please replace this text with the following amended text:

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A5 For the complete surface that is shown in top view in Fig. 11, the layer of polysilicon is the upper layer of dielectric. Areas 42 are the areas of the surface of the substrate over which LOCOS regions have been created, these areas are therefore the areas where the FN tunneling effect takes place and these areas therefore serve as the antenna of the device.

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Q5  
Surface area 40 of polysilicon would typically be the area that is contacted after exposure of the monitoring wafer in order to measure the electron trap out rate. This trap out rate is defined as being the voltage that must be applied between the layer of polysilicon (layer 38, Fig. 10) and the underlying substrate (10, Fig. 10) to induce a 0.1  $\mu$ A current between these two surfaces.

It is clear that if for instance a significant amount of electron charge has taken place, resulting in significant accumulation of FN tunneling electrons in layer 36, Fig. 10, then this voltage is relative small since not much electromagnetic stimulation is required in order to reach a current of 0.1  $\mu$ A[[,]]. The inverse is also true.

The definition of the trap out rate, also referred to as the trap up voltage, can also be stated as follows: the amount of FN voltage that is required to induce a FN current of 0.1  $\mu$ A, where FN refers to the voltage and current as these units relate to the FN layer 36, Fig. 10.

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Q4  
6) page 22, last paragraph, page 23, first paragraph, please replace this text with the following amended text:

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96 Figs. 12a through 12d show four more configurations, using the same numbers for [[the]] highlighting [[of]] the LOCOS regions (42) and the patterned polysilicon (40) as [[has]] have been used [[for]] in Fig. 11. For these configurations, the areas 42, which are the LOCOS regions, are the "collectors" or antenna of the device[[,]]. [[the]] The areas 40, which are the regions of polysilicon, generally serve as the areas that are contacted in order to measure the electron charge effect in accordance with the previously highlighted principles.

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